viciLogic2.0
Online learning and prototyping using PYNQ

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***Abstract*—This demo presents viciLogic2.0, a scalable, distributed, online learning and prototyping platform for gold-standard, basic-to-advanced digital logic design and prototyping education. viciLogic2.0 uses a Xilinx PYNQ [1] reconfigurable System on Chip (SoC) cloud array, and locally-connected SoCs. Client and browser applications provide control and visualisation of the state of all user design signals in real time, within the automatically-allocated and configured remote programmable logic hardware. Each SoC includes an Ethernet-connected ARM-based server which facilitates FPGA resource selection, configuration and control, and remote user interaction. This enables the creation of responsive, interactive client local and browser applications, connected directly to hardware, and online technology enhanced learning applications.**

Keywords—SoC, online learning, FPGA cloud, prototyping, Internet of Things, remote lab, technology enhanced learning

I. INTRODUCTION

The development of advanced, practical skills in digital logic design and reconfigurable SoC/FPGA prototyping is considered challenging and complex. Learners can benefit from access to online hardware, with easy-to-use client-hardware prototyping and application development tools, enabling repeated hands-on practice, and supported by community-driven gold-standard cloud learning. Modern SoCs such as PYNQ [1] and Cyclone-V [2] families provide Internet-of-Things (IoT) capability, which supports online applications. viciLogic is available online (following online registration) [3], along with a range of local and browser viciLogic application demonstrators [4], including (a) online modules from the Fundamentals of Digital Systems course, and (b) a 16-bit single cycle computer (SCC) client application IDE and online lessons.

Figure 1 illustrates the viciLogic2.0 ecosystem, including (a) the traditional user design source project creation and simulation process (for reference), and the viciLogic elements (b) server, (c) FPGA cloud, (d) prototype builder, (e) client local application (with demo view), (f) client browser course application (with demo view). The right hand pane of Figure 1(f) example provides guided online learning to the user, referencing real hardware signal widget-based interaction and visualisation in the left hand pane. Automatic course progression is supported, through monitoring of user widget input and current hardware signal state. Interactive knowledge checks, user sandbox, and interactive timing diagram creation are supported. Figure 2 illustrates a viciLogic client browser course creator application menu extract, corresponding to Figure 1(e) views. The Javascript UI enables tutors to build their own course lessons, linked to their uploaded projects.

II. VICILOGIC2.0 COMPONENTS

This section summarises each of the elements in the viciLogic2.0 ecosystem of Figure 1.

- *Server Controller Registry*, *Figure 1(b)(1):* a central resource management server which transparently configures and allocates an authorised entity, e.g, PYNQ PL (programmable logic), to a requesting client session, based on available authorised resources. Direct client-entity interaction follows the configuration phase, using an allocated controller-entity pair. The controller/entity architecture also supports local hardware connection (via the user's PC Ethernet), and sharable satellite SoC clusters to provide a shared, scalable hardware array.
- *Server Project Repository*, *Figure 1(b)(2):* database of PYNQ SoC bitfile/metadata pairs on the viciLogic server. Users upload projects to the project repository through the Prototype Builder.
- *FPGA Cloud*, *Entity (Fig 1(c)(1)*, *Controller (Fig 1(c)(2))*: an entity is a reconfigurable SoC which executes a project (piece of logic). A controller is an application which manages one or more entities.
- *Prototype Builder*, *Figure 1(d)*: uses a HDL parser/pre-processor and integration of viciLogic core IP block and AXI interconnect to integrate the user design (UD) in the SoC PL and SoC PS components. The generated configuration bitstream supports access to the state of all internal signals in the design, enabling real-time control and visualisation of signals (using widgets). The builder spawns installed vendor EDA tools.
- *Client Local Application Creator*, *Figure 1(e)*: client applications (local and browser) interface with the viciLogic controller registry and controller(s) to program and control entities.
- *Client Browser Application Creator*, *Figure 1(f)*: the Javascript UI creates widget-based application views, using the builder metadata, to enable control and visualisation of user designs. These are available to the course creator application.

III. VICILOGIC USER COMMUNITY

viciLogic offers the following to the community:

- Professors:
  - Online courses and prototyping to support and complement existing courses
  - Sharing of hardware resources through authorised secure networked integration
  - Co-authoring of online courses

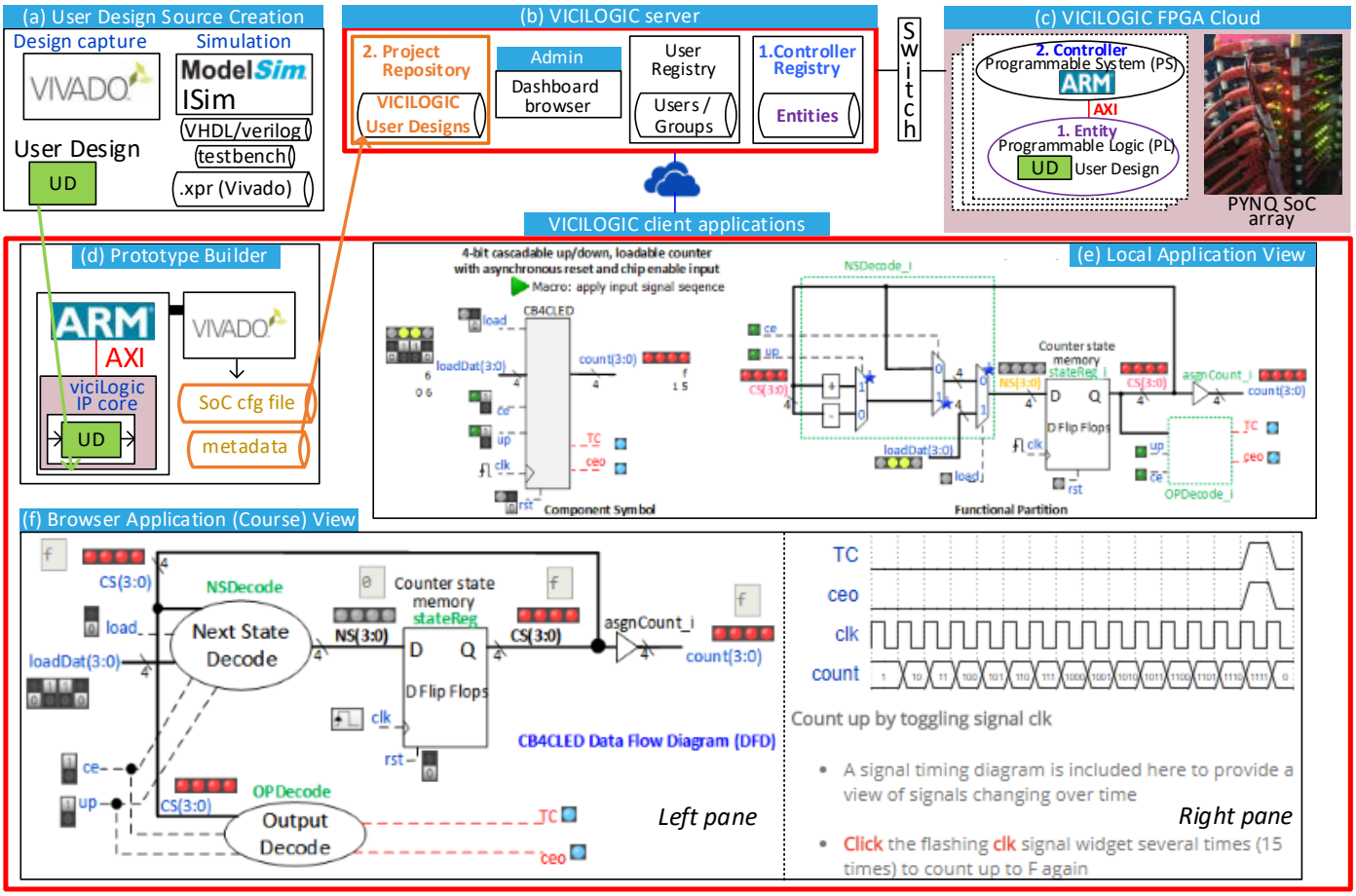

Figure 1 viciLogic2.0 ecosystem, illustrating (a) traditional user design source creation process (for reference), and viciLogic (b) server, (c) FPGA Cloud, (d) prototype builder, (e) client local application (with demo view), (f) client browser course application (with demo view).

- Students
  - Online guided and practical learning-by-doing, with control and visualisation of real hardware
  - Prototyping of lab and project demos
  - Verification testbed for design assignments
- Researchers: component prototyping and demonstrating

The demo illustrates all aspects of the elements in Figure 1. Future work will include (a) pilot application program in a network of universities for the viciLogic Fundamentals of Digital Systems course (b) collaborative development of online courses in processor architectures (SCC and RISC-V), DSP and image processing on FPGA, (c) extending SoC hardware support to Intel Cyclone-V SoC.

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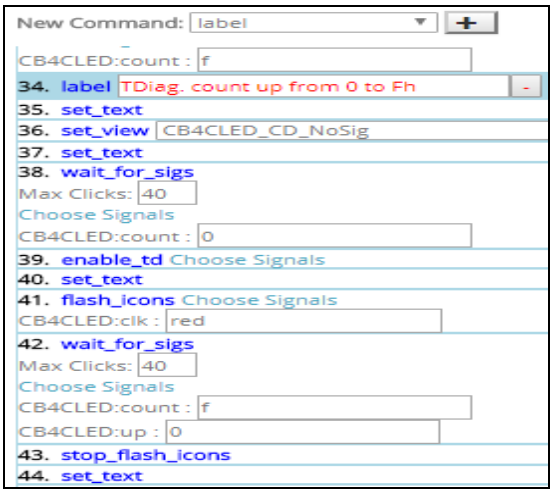

Figure 2 viciLogic client browser course creator command extract

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