Accelerate real-time high-definition video processing designs with Digilent Zybo Z7, a Zynq-7000 AP SoC Platform, Pcam 5C, and Xilinx Vivado HLS

1. Goals:

- Show how to use High Level Synthesis (HLS) to configure the field programmable gate array (FPGA)
- Explain how to build the real-time video processing pipelines and Intellectual Property (IP) in Vivado, the Xilinx computer-aided design (CAD) tool.
- Illustrate the viability of real-time video processing in reconfigurable logic instead of software running on a general-purpose microprocessor.

2. Description:

The workshop keeps in line with Digilent's mission of providing hands-on, project-based, open-ended approach to education. Attendees will use Digilent Zybo Z7, *a Xilinx Zynq SoC FPGA platform*, Pcam 5C, a *5-megapixel MIPI CSI-2 camera sensor* and Xilinx Vivado HLx to implement a real-time high-definition video processing application.

Examples in the workshop materials are based on both high-level programming language (C++) and hardware description language (VHDL). Trainers will demonstrate HLS design flow, IP core usage, simulation and hardware debugging. Participants will leave the workshop with instructional materials and Pcam 5C, a 5-megapixel camera sensor so that they can easily adopt this innovative technique in their own courses and projects.

3. Format: hands-on tutorial in English

4. List of topics covered:

- Explain parallelism, program execution, and performance metrics
- Introduce Xilinx FPGA Architecture and Vivado HLS
- Introduce Digilent Zybo Z7 and Pcam 5C
- Implement video pipeline on Digilent Zybo Z7 and Pcam 5C
- Accelerate video processing algorithm in Xilinx Vivado HLS
- Insert video processing into the pipeline

5. Targeted audience:

The anticipated audience includes faculty members, instructors, laboratory staff, graduate students in the Electronics and Computer Engineering department. Participants need to have basic knowledge about VHDL, C/C++ and digital design.

6. Maximum number of attendees: 25

7. Proposed date & time: 30th August, 09:00-15:30

8. Organizer: Digilent Inc.

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*Local Host at FPL: Robert Owen, Consultant, UK e-mail: Robert.owen@digilent.com tel: +44 1992 584739

9. Speaker:

Elod GYORGY, *Digilent Inc*
Elod GYORGY is the FPGA Engineering Group Manager at Digilent Romania. He has 10 years of experience in embedded hardware design and is familiar with Xilinx technologies. Recently, he has been designing a range of Digilent FPGA SoC platforms powered by Xilinx Zynq and creating tutorials for high level synthesis on Xilinx CAD.

10. Logistics:

- **Hardware:** Digilent will prepare 30pcs Zybo Z7-10 boards, Pcam 5C and USB A to micro-B cables.
- **Required laboratory equipment is 25 workstations with:**
  - Windows 7 at minimum (limited Linux support available)
  - Vivado Design Suite - HLx Edition 2017.4, SDK 2017.4 installed AND licensed (WebPack at least)
  - Monitor with DVI/HDMI input. DVI-to-HDMI cable or HDMI-to-HDMI cable depending on the input available.
- **Visual:** projector and whiteboard available for the presenter.
- **Attendees who to use their own personal computers are responsible for meeting the same technical requirements from above and should contact us in advance.**

11. Previously held

a. RECONF 2017: 20 professors and graduate students attended http://www.ieice.org/~reconf/event/zybo_z7_training_20170927.html -
b. ARC 2018: http://arc2018.esda-lab.cied.teiwest.gr/workshops.html

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